REMARKS

Claims 34-42 are in the application. Claims 1-33 have been cancelled.

By this amendment, applicants have amended claims 34, 39, 41, and 42 to more clearly set forth applicant's invention. FIG. 4 and FIG. 5 support the changes made to the claims.

Response to 35 U.S.C. §112 Rejection

Claims 34-42 were rejected under §112, second paragraph as being indefinite. Specifically, the claimed limitation "a polysilicon having a lower surface" was deemed to be unclear as to whether the lower surface is the same element recited earlier or a different element. Also, the limitation "the lower surface is aligned with the void region" was deemed unclear in claim 34. Additionally, the claimed limitation "contiguous matrix" in claim 41 is unclear as to what the structural difference is between a contiguous matrix and a matrix. Further, the claimed limitation "the lower surface" in claim 42 was deemed unclear as to which lower surface applicants are referring to.

Claim 34 has been amended to remove the two references to the "lower" surface of the polysilicon cap layer so that it is no longer unclear as to whether the surface of the polysilicon cap layer is the same element recited earlier in the claim. The rejection is believed to be overcome by this amendment.

Claim 41 has been amended to remove the term "contiguous matrix." The rejection is believed to be overcome by this amendment.

Claim 42 has been amended to make clear that the lower surface referenced is the lower surface of the first recessed region. The rejection is believed to be overcome by this amendment.

Response to 35 U.S.C. §102 Rejections

Claims 34 and 38-41 were rejected under 35 U.S.C. §102(e) as being anticipated by Lur et al. (USP 5,640,041). This rejection is traversed in view of the amendments made herein and the remarks presented hereinafter.

Claim 34 calls for, among other things, an intermediary of a semiconductor device including a pillar region comprised of a plurality of pillars comprising a dielectric material formed in the first recessed region and extending from the lower surface, wherein a plurality of voids is within the pillar region. Claim 34 also calls for a polysilicon cap layer having a surface formed adjoining upper surfaces of the pillar region and overlying each of the plurality of pillars, wherein the surface of the polysilicon cap layer is aligned with each of the plurality of voids, and wherein sidewall surfaces of the plurality of pillars are devoid of the polysilicon cap layer, and wherein the pillar region and the polysilicon cap layer are configured to form an isolation region having reduced substrate capacitance.

Applicants respectfully submit that Lur does not show nor make obvious a polysilicon cap layer having a surface

formed adjoining upper surfaces of the pillar region and overlying each of the plurality of pillars. Lur shows a structure wherein the polysilicon layer 5 does not overlie each of the plurality of pillars. Some of the pillars in Lur do not have any polysilicon layer 5 overlying them. Thus, Lur does not anticipate applicant's claim 34. Furthermore, applicant's claim 34 calls for the surface of the polysilicon cap layer to be aligned with each of the plurality of voids. Lur also does not show this claimed feature. Lur's polysilicon layer 5 is not aligned with each of the plurality of voids. Lur shows a polysilicon layer 5 which is deposited entirely over numerous voids and not aligned with each void.

The Examiner also states that the claimed limitation of a void region is formed within the pillar region is a process limitation which would carry no patentable weight. This rejection is respectfully traversed. It is not believed that the wording of applicant's claim presented a product by process claim. To remove any ambiguity regarding this issue, applicants have amended the claim to make it clear that a product by process is not claimed. Applicants now claim a "plurality of voids within the pillar region" instead of "a void region is formed within the pillar region." It is now believed to be clear that applicant's claim is not a product by process claim. Thus, for at least these reasons, applicants respectfully submit that claim 34 is allowable.

Claims 38-41 depend from claim 34 and are believed allowable for at least the same reasons as claim 34. The Examiner states that Lur shows a matrix of pillars, however, Lur only states that a "set" of trenches are

formed. Applicants respectfully submit that a set of trenches is not the same as a matrix of a plurality pillars, as claimed by applicants in claim 39.

Claim 41 now calls for the polysilicon cap layer to be aligned with each of the plurality of voids without completely overlying each of the plurality of voids. The polysilicon layer of Lur completely overlies some of the plurality of voids. Thus, for at least the above reasons, applicants respectfully submit that claims 39 and 41 are allowable.

Response to 35 U.S.C. §103 Rejections

Claims 35-37 and 42 were rejected under 35 U.S.C. §103(a) as being unpatentable over Lur. In view of the amendments and arguments presented above and the dependence of these claims on claim 34, applicants respectfully submit that claims 35-37 and 42 are allowable over Lur for at least the same reasons as claim 34. Lur does not make obvious claim 34 because someone skilled in the art would not, with the teaching of Lur, come up with applicant's claimed invention. There is not believed to be any reason or motivation to alter the structure of Lur to make it the same as applicant's claimed structure of claim 34. For at least the above reasons, applicant's claims 35-37 and 42 are believed to be allowable over the relied on reference.

If there are any remaining matters that can be resolved by telephone conference, applicants' undersigned attorney invites Examiner Nadav to contact him at the Examiner's convenience at 602.244.4885.

In view of the above, it is believed that the claims are allowable, and the case is now in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

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